



Information Disclosure Statement

SSN 10/643,772

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LIST OF PATENTS AND PUBLICATIONS STATEMENT	APPLICANTS André DeHon, et al.	
	FILING DATE August 18, 2003	GROUP 2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB- CLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
W	5,144,563	9/1992	Date et al.	364	491	
W	5,796,625	8/1998	Scepanovic et al.	364	491	

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W	Alfke, P., "Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators," Xilinx Application Note, XAPP 052, INTERNET: < http://www.xilinx.com/xapp/xapp203.pdf > pp. 1-6 (July 7, 1996).
	Banerjee, P., Parallel Algorithms for VLSI Computer-Aided Design, Chapter 3, Englewood Cliffs, New Jersey: PTR Prentice Hall, pp. 118-171 (1994).
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EXAMINER 	DATE CONSIDERED 3/2/06
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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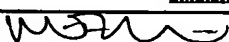
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✓	Sankar, Y., et al., "Trading Quality for Compile Time: Ultra-Fast Placement for FPGAs," <i>Proceedings of the 1999 ACM/SIGDA Seventh International Symposium on Field Programmable Gate Arrays</i> , INTERNET: < http://www.eecg.toronto.edu/~jayar/pubs/sankar/fpga99sankar.pdf > pp. 157-166 (1999).
✓	Schnorr, C.P., et al., "An Optimal Sorting Algorithm For Mesh Connected Computers," presented at the Eighteenth Annual ACM Symposium on Theory of Computing, Berkeley, CA, INTERNET: < http://doi.acm.org/10.1145/359461.359481 > pp. 255-270 (1986).
✓	Shahookar, K., et al., "VSLI Cell Placement Techniques," <i>ACM Computing Surveys (CSUR)</i> , Vol. 23, No. 2, pp.143-220 (June 1991).
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U.S. PATENT DOCUMENTS

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	5,495,419	2/1996	Rostoker et al.	364	468	
	6,243,851 B1	6/2001	Hwang et al.	716	10	
	2003/0174723 A1	9/2003	DeHon et al.	370	404	
	2005/0063373 A1	3/2005	DeHon et al.	370	380	

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	PUBLICATION DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
98/35294	8/1998	WO			abstract

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WD	Arora, S., et al., "On-Line Algorithms For Path Selection In A Nonblocking Network," <i>SIAM Journal on Computing</i> , Vol. 25, No. 3, pp. 1-25 (June 1996).
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WD	Bhatt, S.N., et al., "A Framework for Solving VLSI Graph Layout Problems," <i>Journal of Computer and System Sciences</i> , Vol. 28, pp. 300-345 (1984).
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ND	DeHon, A., "Compact, Multilayer Layout for Butterfly Fat-Tree," <i>Proceedings of the Twelfth ACM Symposium on Parallel Algorithms and Architectures</i> , 10 pages total (July 2000).
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